REMARKS

Claim 18 is cancelled as being redundant with claim 1. Claims 1-7, 9, 11-17, and 19-20 are pending in this application. Reconsideration and allowance of the application are respectfully requested. In the discussion set forth below, Applicants do not acquiesce to any rejection or averment in the Office Action unless expressly indicated.

Non-obviousness over the Lulla-Geer-Aralis combination

Claims 1-2, 4-5, 9, 15, 17 and 19-20 are understood to be patentable under 35 USC §103(a) over "Lulla" (U.S. Patent No. 6,922,820 to Lulla et al.), in view of "Geer" (U.S. Patent No. 5,079,725 to Geer), and further in view of "Aralis" (U.S. Patent No. 5,319,598 to Aralis et al.). The rejection is respectfully traversed because the Examiner has not shown that all the features are suggested by the combination and has not provided a proper motivation for modifying the teachings of Lulla with teachings of Geer and Aralis.

The method of claim 1 for identifying and configuring a system includes, among other limitations generating a first system identifier value that identifies a first system as a function of values read from and respective positions of a first plurality of devices in a scan chain, generating a target system identifier value that identifies the target system as a function of the values read from a second plurality of devices in a target system and respective positions of the second plurality of devices in a scan chain, comparing the first system identifier value to the target system identifier value, configuring the second plurality of devices in the target system if the system identifiers match, and halting the configuring if the system identifier values do not match. Applicants respectfully submit that the Lulla-Geer-Aralis combination neither teaches nor suggests the claimed generating of any system identifier value nor the claimed use thereof.

The Examiner cited certain elements of each of Lulla, Geer, and Aralis as corresponding to certain claim limitations. Thus, the asserted correspondences to the

claim limitations are discussed individually in the paragraphs that follow. The Examiner asserted the following correspondences:

Lulla: reading identification codes from first plurality of devices, and generating a first system identifier from the values of the identification codes;
Geer: a plurality of devices in a scan chain and the first system identifier being generated as a function of positions of the first plurality of devices; and
Aralis: storing the first system identifier value with respective configuration data sets of the first plurality of devices, reading identification codes from a second plurality of devices, generating a target system identifier value from the identification codes from a second plurality of devices and respective positions, comparing the target and first system identifier values, and configuring or halting the configuring based on the comparison.

Lulla neither teaches nor suggests reading identification codes from a first plurality of devices, and generating a first system identifier from the values of the identification codes. Lulla generally teaches use of unique identification codes for different devices (col. 1, ll. 55-58). Lulla's invention is a circuit that selects one of a number of ID codes in response to a voltage level at each of a number of pins of the device (col. 1, l. 65 – col. 2, l. 2). Lulla teaches a device with an ID code register having a portion for storing a version number of the device, a portion for storing a manufacturing number of the device, a portion that indicates that the register is present, and a portion to indicate a part number (col. 2, l. 64 – col. 3, l. 14). Lulla further teaches that the portions of the ID code register may be programmed with a logic circuit that is responsive to the voltage levels at a number of pins of the device (FIG. 3, FIG. 4; col. 3, ll. 36-50).

Those skilled in the art would not recognize Lulla's portions 102-108 as being equivalent to the first plurality of devices of a system as the Examiner asserts. The cited portions 102-108 are expressly described by Lulla as being a register 100 (FIG. 3; col. 2, line 64-65). Lully also expressly indicates that the register is part of a single device 90 (FIG. 3; col. 2, line 64). The portions 102-108 of the register store data that indicate a version number for the IC, a manufacturing number, the presence of the register in the particular IC, and a part number of the IC (col. 3, lines 1-12). Thus, Lulla's express teachings are at odds with the Examiner's assertion of the register portions being equivalent to the claimed plurality of devices, and Lulla's teachings for

the ID code register do not suggest either reading identification codes from the first plurality of devices, or generating a first system identifier from the values of the identification codes.

Geer neither teaches nor suggests the first system identifier being generated as a function of positions of the first plurality of devices on the scan chain. Geer generally teaches a predetermined identification number being assigned to each chip to be identified (Abstract). Geer teaches that shift register latches (SRLs) may be used in a scan ring on a chip to store chip ID bits and level ID bits (col. 3, ll. 1-12). In an alternative, Geer teaches that certain ones of the SRLs could store bits that indicate a location of other SRLs on the same chip from which an identification number may be retrieved (col. 5, ll. 29-35).

The Examiner asserts that retrieving an identification number as taught by Geer is equivalent to the claimed generating the system identifier since Geer teaches that some SRLs may store the location of other SRLs from which the identification number may be retrieved. Applicants respectfully submit that Geer's SRLs storing of other SRL locations is not equivalent to the claimed generating the system identifier.

Geer's teachings, similar to Lulla's teachings, are directed to the identification of a single chip/IC/device. Geer clearly indicates that "the assigned predetermined identification number is stored in a plurality of predefined shift register latches (SRLs) in the LSI chip to be identified [and] the LSI ship is identified by reading out the stored predetermined identification number" (col. 2, ll. 26-31). Geer does not suggest generating a first system identifier value from a plurality of chip IDs (and/or level IDs) from multiple chips and the positions of those chips on a scan chain. Thus, Geer's teachings for the SLRs containing chip/level IDs for a single chip neither teach nor suggests the first system identifier being generated as a function of positions of the first plurality of devices in a scan chain.

Aralis neither teaches nor suggests the reading of identification codes from a second plurality of devices, generating a target system identifier value from the identification codes from the second plurality of devices and respective positions in the scan chain, comparing the target and first system identifier values, and configuring or halting the configuring based on the comparison.

Aralis generally teaches a configuration control serial interface for controlling the configuration of a solid state dip switch for a particular circuit (FIG. 1; col. 2, ll. 17-23). "According to a feature of [Aralis'] invention a configurable circuit has its configuration controlled by a nonvolatile memory, and one of a plurality of such configurable circuits is selected by matching the circuit ID code with an interrogation code." (col. 1, ll. 59-63). More particularly, Aralis teaches that the configuration control serial interface for a circuit includes a ID code memory/register and a programmable non-volatile memory. If an interrogation code shifted into the configuration control serial interface matches the circuit ID code stored in the ID code memory/register, the configuration control serial interface loads shifted-in serial data into the programmable non-volatile memory (col. 2, l. 56 – col. 3, l. 10; col. 4, ll. 26-55).

Aralis contains further teachings in regards to a chain of devices (FIG. 4; col. 7, l. 47 – col. 8, l. 63). However, Aralis' teachings for a chain of devices does not suggest the claimed reading of identification codes from a second plurality of devices, generating a target system identifier value from the identification codes from the second plurality of devices and respective positions in the scan chain, comparing the target and first system identifier values, and configuring or halting the configuring based on the comparison. To program a new configuration into selected device(s) on the chain, Aralis teaches reading the ID codes from a chain of devices in order to learn the proper ID code(s). The correct device ID code(s) and programming data are shifted into the chain of devices and programming is enabled as described above.

Aralis has no apparent need for the single target system identifier value that is generated as a function of all the values read from the plurality of devices. Rather, Aralis uses only the individual device identifiers to program individual devices. Thus, Aralis teaching of the programmable solid-state dip switches in a scan chain does not suggest any generating of a target system identifier value from the identification codes from the second plurality of devices and respective positions of those devices in the scan chain.

The asserted motivation for modifying Lull with teachings of Geer is unsupported by evidence and improper. The Examiner stated that "it would have been obvious … to improve upon the method of Lulla … because it would provide Lulla's

method with the enhanced capability of uniquely identifying integrated circuit chips adapted for use with scan design system and scan testing techniques." Applicants respectfully submit that Lulla, without Geer's teachings, employs boundary scan techniques and also uniquely identifies circuits (col. 2, ll. 35-63). In addition, there has been no evidence presented that shows Lulla is in any manner deficient or that shows how Lulla would be improved by Geer's teachings. Therefore, the asserted motivation is unsupported by evidence and improper.

The asserted motivation for modifying Lulla with teachings of Aralis is unsupported by evidence and improper. The Examiner stated that "it would have been obvious … to improve upon the method of Lulla …because it would provide the modified Lulla with the enhanced capability of providing configurable circuits which may be difficult to access." Applicants respectfully submit that Lulla, without Aralis' teachings, provides unique identification of PLD circuits (Title; col. 2, ll. 3-11). Since PLDs are configurable, Lulla provides identification of configurable circuits. In addition, there has been no evidence presented that shows Lulla is in any manner deficient or that shows how Lulla would be improved by Aralis' teachings. Therefore, the asserted motivation is unsupported by evidence and improper.

Applicants submit that independent claims 19 and 20 are patentable over the cited references for reasons similar to those provided above with respect to claim 1; claims 2, 4-5, 9, 15, and 17 have claim 1 as a base claim. Therefore, the Examiner has not shown that the Lulla-Geer-Aralis combination suggests all the limitations of these claims and the motivations for making the combination is improper for at least the reasons set forth above.

The rejection of claims 1-2, 4-5, 9, 15, 17 and 19-20 should be withdrawn because a *prima facie* case of obviousness has not been established.

Non-obviousness over the Lulla-Geer-Aralis-Dreyer combination

Claim 3 is understood to be patentable under 35 USC §103(a) over the Lulla-Geer-Aralis combination, further in view of "Dreyer" (U.S. Patent No. 5,794,066 to Dreyer et al.). The rejection is respectfully traversed because a *prima facie* case of obviousness has not been established. Claim 3 has claim 1 as a base claim, and

Dreyer does not remedy the deficiencies of the Lulla-Geer-Aralis combination as applied to claim 1. Therefore, the rejection of claim 3 should be withdrawn.

Non-obviousness over the Lulla-Geer-Aralis-Jacobson combination

Claims 6-7 and 16 are understood to be patentable under 35 USC §103(a) over the Lulla-Geer-Aralis combination, further in view of "Jacobson" (U.S. Patent No. 5,841,867 to Jacobson et al.). The rejection is respectfully traversed because a *prima facie* case of obviousness has not been established. Claims 6-7 and 16 have claim 1 as a base claim, and Jacobson does not remedy the deficiencies of the Lulla-Geer-Aralis combination as applied to claim 1. Therefore, the rejection of claims 6-7 and 16 should be withdrawn.

Non-obviousness over the Lulla-Geer-Aralis-IBM combination

Claim 11 is understood to be patentable under 35 USC §103(a) over the Lulla-Geer-Aralis combination, further in view of "IBM" (IBM Technical Disclosure Bulletin (IBM), NA8909262). The rejection is respectfully traversed because a *prima facie* case of obviousness has not been established. Claim 11 has claim 1 as a base claim, and IBM does not remedy the deficiencies of the Lulla-Geer-Aralis combination as applied to claim 1. Therefore, the rejection of claim 11 should be withdrawn.

Non-obviousness over the Lulla-Geer-Aralis-IBM-Jacobson combination

Claims 11-14 are understood to be patentable under 35 USC §103(a) over the Lulla-Geer-Aralis-IBM combination, further in view of Jacobson. The rejection is respectfully traversed because a *prima facie* case of obviousness has not been established. Claims 12-14 have claim 1 as a base claim, and Jacobson does not remedy the deficiencies of the Lulla-Geer-Aralis combination as applied to claim 1. Therefore, the rejection of claims 12-14 should be withdrawn.

Non-obviousness over the Lulla-Geer-Aralis-Thiel combination

The rejection of claim 18 under 35 USC §103(a) over the Lulla-Geer combination, further in view of "Thiel" (U.S. Patent No. 6,381,509 to Thiel et al.) is respectfully traversed. However, the rejection is moot in view of the cancellation of claim 18.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call is invited to the undersigned at (408) 879-4682.

Respectfully submitted,

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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent & Trademark Office on January 9, 2009.

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